

METHOD FOR MANUFACTURING CAPACITOR BOTTOM
ELECTRODE OF SEMICONDUCTOR DEVICE

Field of the Invention

5

The present invention relates to a method for manufacturing a semiconductor device; and, more particularly, to a method for manufacturing a capacitor bottom electrode of the semiconductor device using a dielectric material with a low dielectric constant (low k dielectric) as a sacrificial layer, thereby simplifying a manufacturing process and enhancing a capacitor property.

Description of the Prior Art

15

As is well known, a semiconductor device has been downsized by a scale down of a design rule. Therefore, various researches have been conducted for securing charge storage capacity according to micronization. To fabricate a capacitor with three-dimensional structure such as a concave type and a stack type, is also one of the methods for securing storage capacity.

20

There are provided in Figs. 1A to 1G cross sectional views setting forth a conventional method for manufacturing a capacitor bottom electrode with the concave type for use in the semiconductor device.

25

Referring to Fig. 1A, the conventional method for

manufacturing the capacitor bottom electrode begins with preparing a semiconductor substrate 110. Thereafter, a first insulating layer 112 is formed on a top face of the semiconductor substrate 110 and then is patterned into a first predetermined configuration to form a first contact plug 114, wherein the first contact plug 114 is electrically connected to an active area, e.g., source/drain regions of the semiconductor substrate 110 which are not depicted in the drawing for the sake of convenience.

Here, Tetraethyl Ortho Silicate (TEOS) layer is used for the first insulating layer 112 and the first contact plug 114 is polysilicon. On the top face of the first contact plug 114, additionally, a barrier layer (not shown) of Ti/TiSi₂/TiN structure may be formed in order to prevent diffusion phenomenon.

Subsequently, top faces of the first contact plug 114 and the first insulating layer 112 are planarized by using a chemical mechanical polishing (CMP) process. Then, a second insulating layer 116 is formed on planarized top faces of the first contact plug 114 and the first insulating layer 112.

In a next step, bit lines 118 are formed on portions of the second insulating layer 116, wherein the bit lines 118 and the first contact plug 114 are not overlapped each other. Thereafter, an etch stop layer 120 is deposited on exposed surfaces of the bit lines 118 and the second insulating layer 116.

The first etch stop layer 120 plays a role in preventing

loss of the bit lines 118 during a post etching process for forming a storage node contact of a capacitor. Especially, a nitride layer such as silicon nitride layer and silicon oxynitride layer, can be used as the etch stop layer 120 for
5 securing etching selectivity with respect to a third insulating layer 122, i.e., an oxidation layer.

Next, the third insulating layer 122 is formed on the first etch stop layer 120 and is planarized by using a method such as an etchback process and the CMP process.

10 Thereafter, a first photoresist layer is formed on the third insulating layer 122 and is patterned into a second predetermined configuration in order to form the storage node contact, thereby obtaining a first photoresist pattern 124 as shown in Fig. 1A.

15 In an ensuing step, the third insulating layer 122, the first etch stop layer 120 and the second insulating layer 116 are successively patterned into a third predetermined configuration till the top face of the first contact plug 114 is exposed, whereby a contact hole (not shown) is formed.
20 Here, the first etch stop layer 120 and the second insulating layer 116 are etched after the third insulating layer 122 is etched. Thus, a desired etch profile can be achieved by modulating an etching recipe for each etching step.

25 In a subsequent step as shown in Fig. 1B, plug material such as polysilicon is filled in the contact hole and is planarized by the CMP process so that a second contact plug 126 is formed, wherein the first contact plug 114 and the

second contact plug 126 are electrically connected to each other. Here, the second plug 126 is referred to as the storage node contact.

Referring to Fig. 1C, subsequently, a second etch stop layer 128, e.g., a nitride layer is formed on top faces of the second contact plug 126 and the third insulating layer 122 to prevent a damage of the second plug 126 during a post etching step for forming a capacitor bottom electrode 134. Next, a sacrificial layer 130 is formed on the top face of the second etch stop layer 128 with a predetermined thickness in consideration of the height of the designed capacitor. Then, a second photoresist layer is formed on the sacrificial layer 130 and is patterned into a fourth predetermined configuration so that a second photoresist pattern 132 is formed.

Thereafter, the sacrificial layer 130 is patterned using the second photoresist pattern 132 as an etching mask. A first etching step is carried out till the top face of the second etch stop layer 128 is exposed and a second etching step is carried out till the top face of the second plug 126 is exposed, thereby obtaining an opening 131. Here, polysilicon may be used as a hard mask between the sacrificial layer 130 and the second photoresist pattern 132. Then, the second photoresist pattern 132 is removed as shown in Fig. 1D.

In a next step as shown in Fig. 1E, a conductive layer 132 is deposited over the resultant structure including the opening 132 with uniform thickness so that the conductive layer 132 is electrically connected to the second contact plug

126. After forming the conductive layer 132, a photoresist is deposited to fill a concave part of the conductive layer 132 completely.

5 In an ensuing step, as shown in Fig. 1F, the conductive layer 132 is planarized using a method such as the etchback process and the CMP process till the top face of the sacrificial layer 130 is exposed, whereby the conductive layer 132 remains only in the concave part thereof.

10 Subsequently, residuals of the sacrificial layer 130 are cleared off by means of a wet dip-out process using buffered oxide etchant (BOE) or hydrogen fluoride (HF) acid. Thereafter, the residual photoresist layer 134A is removed by means of a dry strip process. That is, the residual photoresist 134A and by-products produced during the etching
15 step are removed by means of rinse of solvent, after the photoresist layer is etched using $O_2/CF_4/H_2O/N_2$ or O_2/N_2 . Thus, a bottom electrode 132A with a concave type is achieved as shown in Fig. 1G.

20 In a next step, an annealing process is carried out for recovering a deteriorated characteristic of the bottom electrode 132A incurred during the etching process. Then, residual impurity is removed by a rinse-out process using solution like BOE before forming a dielectric layer on the bottom electrode 132A.

25 Finally, as not shown in drawings, the dielectric layer and a top electrode are formed on the bottom electrode 132A subsequently, whereby the capacitor is fabricated.

Referring to Fig. 2, there is a plane view of a plurality of the capacitors arranged on the semiconductor substrate 110 according to the conventional method for manufacturing the bottom electrode 132A.

5 In Fig. 2, a plurality of bottom electrodes 132A are arranged to a predetermined orientation and a plurality of second contact plugs 126 are arranged between bit lines 118 like a matrix. Each bottom electrode 132A is overlapped each second plug 126, wherein each bottom electrode 132A are
10 electrically connected to each second plug 126.

Meanwhile, the bottom electrode 132A is formed by etching the sacrificial layer 130 using a rectangular typed mask or an ellipsoidal typed mask up to date. In this case, there is happened a problem that adjacent bottom electrodes 132A are
15 apt to cling together due to a surface tension of HF acid or BOE solution during the wet dip-out process, thereby incurring an electrical shortage between the adjacent bottom electrodes 132A.

Referring to Fig. 3, there is a cross sectional view
20 setting forth a shortage phenomenon 140 between the adjacent bottom electrodes 132A according to the conventional method for manufacturing the capacitor. As distance (d) between the adjacent bottom electrodes 132A is shortened and an adjacent area increases, the shortage phenomenon 140 is more serious.
25 Furthermore, as the bottom electrode 132A becomes narrow and high, the shortage phenomenon 140 is also happened seriously.

Additionally, as a vertical dimension of the capacitor

increases, a process margin decreases due to a gap-fill property while forming a metal contact and a barrier layer, thereby increasing contact resistance in the long run. According to the prior art method, the process for forming the bottom electrode 132A is so complicated, to thereby increase a manufacturing cost. That is, in order to form the bottom electrode 132A in the prior art, it is necessary to carry out a series of process for forming the etch stop layer, the polysilicon grain (PSG) layer, a plasma enhanced TEOS (PE-TEOS) layer, the hard mask and the photoresist layer. Therefore, in order to reduce the manufacturing cost, it should be necessary to solve the shortage problem 140 between the adjacent bottom electrodes 132A and to simplify the manufacturing process.

Summary of the Invention

It is, therefore, an object of the present invention to provide a method for manufacturing a capacitor bottom electrode of the semiconductor memory device using a low k dielectric layer as a sacrificial layer, thereby simplifying manufacturing process and enhancing a capacitor property.

In accordance with one aspect of the present invention, there is provided a method for manufacturing a capacitor bottom electrode of a semiconductor device, the method including the steps of: a) preparing a semiconductor substrate obtained by a predetermined process; b) forming a sacrificial

layer of low k dielectric material on the semiconductor substrate; c) forming a photoresist pattern on the sacrificial layer; d) etching the sacrificial layer by using the photoresist pattern as an etching mask, thereby forming an opening; e) depositing a conductive layer on sides and a bottom face of the opening and a top face of the sacrificial layer; f) forming a photoresist on the conductive layer, wherein a concave region of the conductive layer is completely filled with the photoresist; g) planarizing the conductive layer till a top face of the sacrificial layer is exposed; and h) forming a bottom electrode by removing the sacrificial layer enclosing the bottom electrode by using O₂ plasma and by removing a residual photoresist.

Brief Description of the Drawings

The above and other objects and features of the present invention will become apparent from the following description of the preferred embodiments given in conjunction with the accompanying drawings, in which:

Figs. 1A to 1G are cross sectional views setting forth a conventional method for manufacturing a bottom electrode with a concave type for use in a semiconductor device;

Fig. 2 is a plane view of a plurality of the capacitors arranged on a semiconductor substrate according to the conventional method for manufacturing the bottom electrode with the concave type;

Fig. 3 is a cross sectional view setting forth a shortage phenomenon between adjacent bottom electrodes of the conventional method; and

Figs. 4A to 4G are cross sectional views setting forth a method for manufacturing the bottom electrode with the concave type in accordance with a preferred embodiment of the present invention.

Detailed Description of the Preferred Embodiments

There are provided in Figs. 4A to 4G cross sectional views setting forth a method for manufacturing a capacitor bottom electrode with a concave type for use in a capacitor in accordance with a preferred embodiment of the present invention.

Referring to Fig. 4A, the inventive method for manufacturing the bottom electrode begins with preparation of a semiconductor substrate 210. Thereafter, a first insulating layer 212 is formed on a top face of the semiconductor substrate 210 and then, is patterned into a first predetermined configuration to form a first contact plug 214, wherein the first contact plug 214 is electrically connected to source/drain regions of the semiconductor substrate 210 which are shown in the drawing.

Here, Tetraethyl Ortho Silicate (TEOS) layer is used for the first insulating layer 212 and the first contact plug 214 is polysilicon. On the top face of the first contact plug

214, additionally, a barrier layer (not shown) of Ti/TiSi₂/TiN or Ti/TiN structure can be formed in order to prevent diffusion phenomenon.

5 Subsequently, top faces of the first contact plug 214 and the first insulating layer 212 are planarized by using a chemical mechanical polishing (CMP) process. Then, a second insulating layer 216 is formed on planarized top faces of the first contact plug 214 and the first insulating layer 212.

10 In a next step, bit lines 218 are formed on portions of the second insulating layer 216, wherein the bit lines 218 and the first contact plug 214 are not overlapped each other. Thereafter, an etch stop layer 220 such as a nitride layer is deposited on exposed surfaces of the bit lines 218 and the second insulating layer 216.

15 The etch stop layer 220 plays a role in preventing loss of the bit lines 218 during a post etching process for forming a storage node contact of a capacitor. Especially, the nitride layer such as a silicon nitride layer and an silicon oxy-nitride layer, can be used as the etch stop layer 220 for
20 securing etching selectivity with respect to a third insulating layer 222, i.e., an oxidation layer.

Next, the third insulating layer 222 is formed on the etch stop layer 220 and is planarized by using a method such as an etchback process and the CMP process.

25 Thereafter, a first photoresist pattern (not shown) is formed predetermined top faces of the third insulating layer 222. Then, the third insulating layer 222, the first etch

stop layer 220 and the second insulating layer 216 are successively patterned into a third predetermined configuration using the first photoresist pattern as a mask till the top face of the first contact plug 114 is exposed, whereby a contact hole (not shown) is formed. Namely, the third insulating layer 222 is etched till the top face of the etch stop layer 220 is exposed and then the etch stop layer 220 and the second insulating layer 216 are etched, thereby obtaining a desired vertical etching profile.

In a subsequent step, conductive material such as polysilicon is filled in the contact hole and is planarized by the CMP process so that a second contact plug 226 is formed, wherein the first contact plug 214 and the second contact plug 226 are electrically connected to each other. Here, the second plug 226 is referred to as the storage node contact.

Subsequently, a sacrificial layer 228 is formed on the second contact plug 226 with a predetermined thickness in consideration of the height of the designed capacitor. Here, the inventive method employs an organic material or an inorganic material with low dielectric constant, i.e., low k , as the sacrificial layer 228. Then, a second photoresist layer is formed on the sacrificial layer 228 and is patterned into a fourth predetermined configuration so that a second photoresist pattern 230 is formed as shown in Fig. 4B.

Thereafter, referring to Fig. 4C, the sacrificial layer 228 is patterned by using the second photoresist pattern 230 as the mask. That is, the sacrificial layer 228 is etched

making use of the photoresist pattern 230 as an etching mask till the top face of the second contact plug 226 is exposed, whereby an opening 229 is obtained. In an ensuing step, the photoresist pattern 230 is removed through a photoresist strip
5 process.

In order to obtain a vertical profile of the etched section, it is preferable that it should be to use hydrocarbon gas such as N_2 and C_2H_4 or hydro-fluoro gas such as C_4F_8 , C_5F_8 and C_4F_6 . In addition, it is preferable to add small
10 amount of oxygen gas for obtaining etching selectivity with respect to the second photoresist pattern 230.

Subsequently, a conductive layer 232 is deposited over the resultant structure including the opening 229 with uniform thickness, wherein the conductive layer 232 and the second
15 contact plug 226 are electrically connected to each other, as shown in Fig. 4D.

In a next step as shown in Fig. 4E, photoresist material is filled in a concave region 229A of the conductive layer 232. It is preferable that the material for use in the
20 conductive layer 232 should be selected from the group consisting of polysilicon, tungsten, titanium nitride (TiN), tungsten silicide and the combination thereof, by using an atomic layer deposition (ALD) method. In the conventional method, polysilicon is used for the conductive layer 232,
25 which is deposited using a conventional furnace.

Thereafter, the conductive layer 232 is planarized using a method such as the etchback process or the CMP process till

the top face of the sacrificial layer 228 is exposed, whereby the conductive layer 232 remains only in the concave region 229A thereof, as depicted in Fig. 4F. In the etchback process, Cl_2 and BCl_3 gas is used as basic gas for plasma gas.

5 However, since it is necessary to use oxygen gas during the process for removing the sacrificial layer 228, it is preferable to add oxygen gas to Cl_2 and BCl_3 gas simultaneously in order to reduce the process time. Also, SF_6/N_2 gas can be used as basic gas for plasma gas, which is
10 conventionally used for etching tungsten or tungsten silicide. Like using Cl_2 and BCl_3 gas as basic gas for the etchback process, it is preferable to use mixture gas of basic SF_6/N_2 gas and supplementary O_2 gas for reducing the process time.

Thereafter, the removal of the sacrificial layer 228 is
15 carried out not using the conventional wet dip-out process but using a dry process by virtue of plasma. Here, since oxygen gas is good for removing low K dielectric layer, oxygen gas is utilized for plasma gas to remove the sacrificial layer 228. In this case, it is preferable that it should be to use N_2 ,
20 H_2 , CF_4 and NF_3 plasma gas with O_2 plasma gas for a surface treatment.

After finishing the process for removing the sacrificial layer 228, the residual photoresist 234A is removed by a dry strip process so that the bottom electrode manufactured by the
25 inventive method is obtained as shown in Fig. 4G. That is, after the photoresist 234 is etched using $\text{O}_2/\text{CF}_4/\text{H}_2\text{O}/\text{N}_2$ or O_2/N_2 , the residual photoresist 234A and the by-product

produced in the etching step is rinsed out by means of solvent.

Subsequently, an annealing process may be carried out for recovering the deteriorated property of the bottom electrode 232A incurred during the etching step. At this time, impurity is cleared off using BOE solution before forming a dielectric layer on the bottom electrode 232A.

Meanwhile, in case of forming the bottom electrode 232A using a metastable polysilicon (MPS) process, the MPS grain can be grown up upon the inner side of the bottom electrode 232A in an ambient of a predetermined temperature and pressure after the depositing polysilicon on the bottom electrode 232A. After this, the top face of the bottom electrode 232A is planarized through the CMP process.

Finally, as is not shown in the drawing, a dielectric layer and a top electrode are formed on the bottom electrode subsequently.

In comparison with the prior art, polysilicon has been used for the hard mask in the prior art method because the oxidation layer is too strong to be patterned. Thus, it is difficult to use the photoresist as the mask. In addition, since it is possible to etch the oxidation layer by a physical attack of ions in plasma gas, the bottom region of the opening 229 is narrower than the top region of the opening 229. This phenomenon is called "Ion Shadowing Effect".

Therefore, in fabrication of the semiconductor device having minimal linewidth of 0.13 μm , double oxidation layer of

phosphosilicate glass (PSG) and plasma enhanced TEOS (PE-TEOS) is utilized as the third insulating layer 222. Therefore, it is necessary to carry out the supplementary process for broadening the bottom region of the opening and removing the polysilicon hard mask.

In the present invention, however, the sacrificial layer 228 uses low k dielectric material which is not strong in comparison with the oxidation layer, whereby it is not necessary to use polysilicon as the hard mask. Additionally, it is easy to secure the bottom area of the opening 229 owing to the strong chemical characteristic in accordance with the present invention.

In the prior art method, the removal of the oxidation layer, i.e., the sacrificial layer 228, can be performed by the wet dip-out process. But, in the present invention, O₂ plasma is utilized for removing the sacrificial layer 228 so that it is possible to overcome the shortage phenomenon between the adjacent bottom electrodes 232A caused by the surface tension during the wet dip-out process. Thus, it is possible to achieve a semiconductor capacitor with an enhanced electrical property.

As aforementioned, since the low k dielectric material is used as the sacrificial layer 228 for manufacturing the capacitor bottom electrode in the present invention, it is possible to abbreviate the process for forming the hard mask and the process for forming the etch stop layer so that the fabrication process can be simplified..

While the present invention has been described with respect to the particular embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of
5 the invention as defined in the following claims.